




ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	ASYNCHRONOUS SYSTEM-ON-A-CHIP INTERCONNECT						
Application Number: 10/634597							
Confirmation Number: 6534							
First Named Applicant: URI CUMMINGS							
Attorney Docket Number: FULCP009							
Art Unit: 2631							
Search string: (6230228 or 5802055 or 6279065 or 6301630).pn.							
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
KCT	1	6230228	2001-05-08	Eskandari et al.		710	129
KCT	2	5802055	1998-09-01	Krein et al.		370	402
KCT	3	6279065	2001-08-21	Chin et al.		710	129
KCT	4	6301630	2001-10-09	Chen et al.		710	129
Signature							
Examiner Name				Date			
Frank Wong Tran				08/19/2004			



Form 1449 (Modified)	Atty Docket No. FULCP009	Application No.: 10/634,597
Information Disclosure Statement By Applicant	Applicant: Cummings et al.	
(Use Several Sheets if Necessary)	Filing Date August 4, 2003	Group Not yet assigned

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
KCT	A	6,038,656	03.14.00	Martin et al.			
KCT	B	5,752,070	05.12.98	Martin et al.			
KCT	C	6,044,061	03.28.00	Aybay et al.			
KCT	D	5,832,303	11.03.98	Murase et al.			

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
KCT	E	Andrew Matthew Lines, <u>Pipelined Asynchronous Circuits</u> , June 1995, revised June 1998, pp. 1-37.
KCT	F	Alain J. Martin, <u>Compiling Communicating Processes into Delay-Insensitive VLSI Circuits</u> , December 31, 1985, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-16.
KCT	G	Alain J. Martin, <u>Erratum: Synthesis of Asynchronous VLSI Circuits</u> , March 22, 2000, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-143.
KCT	H	U.V. Cummings, et al. <u>An Asynchronous Pipelined Lattice Structure Filter</u> , Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-8.
KCT	I	Alain J. Martin, et al. <u>The Design of an Asynchronous MIPS R3000 Microprocessor</u> , Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-18.
KCT	J	C.L. Seitz, <u>System Timing</u> , chapter 7, pp. 218-262.
KCT	K	F.U. Rosemberger et al., <u>Internally Clocked Delay-Insensitive Modules</u> , IEEE Trans., Computers, vol. 37, no. 9, pp. 1005-1018, September 1998.
KCT	L	U.S. Application 09/501,638, filed on February 10, 2000, entitled, <u>Reshuffled Communications Processes in Pipelined Asynchronous Circuits</u> .
KCT	M	Lee et al., <u>Crossbar-Based Gigabit Packet Switch with an Input-Polling Shared Bus Arbitration Mechanism</u> , September 21, 1997, XVI World Telecom Congress Proceedings, Interactive Session 3 - Systems Technology & Engineering, pp. 435-441.
KCT	N	Ghosh et al., <u>Distributed Control Schemes for Fast Arbitration in Large Crossbar Networks</u> , March 1994, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 1, pp. 55-67.
Examiner	Khanh Cong Tran	
	Date Considered	08/19/2004

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered Include copy of this form with next communication to applicant.